The Two-Channel Transistor for Low-Energy Applications

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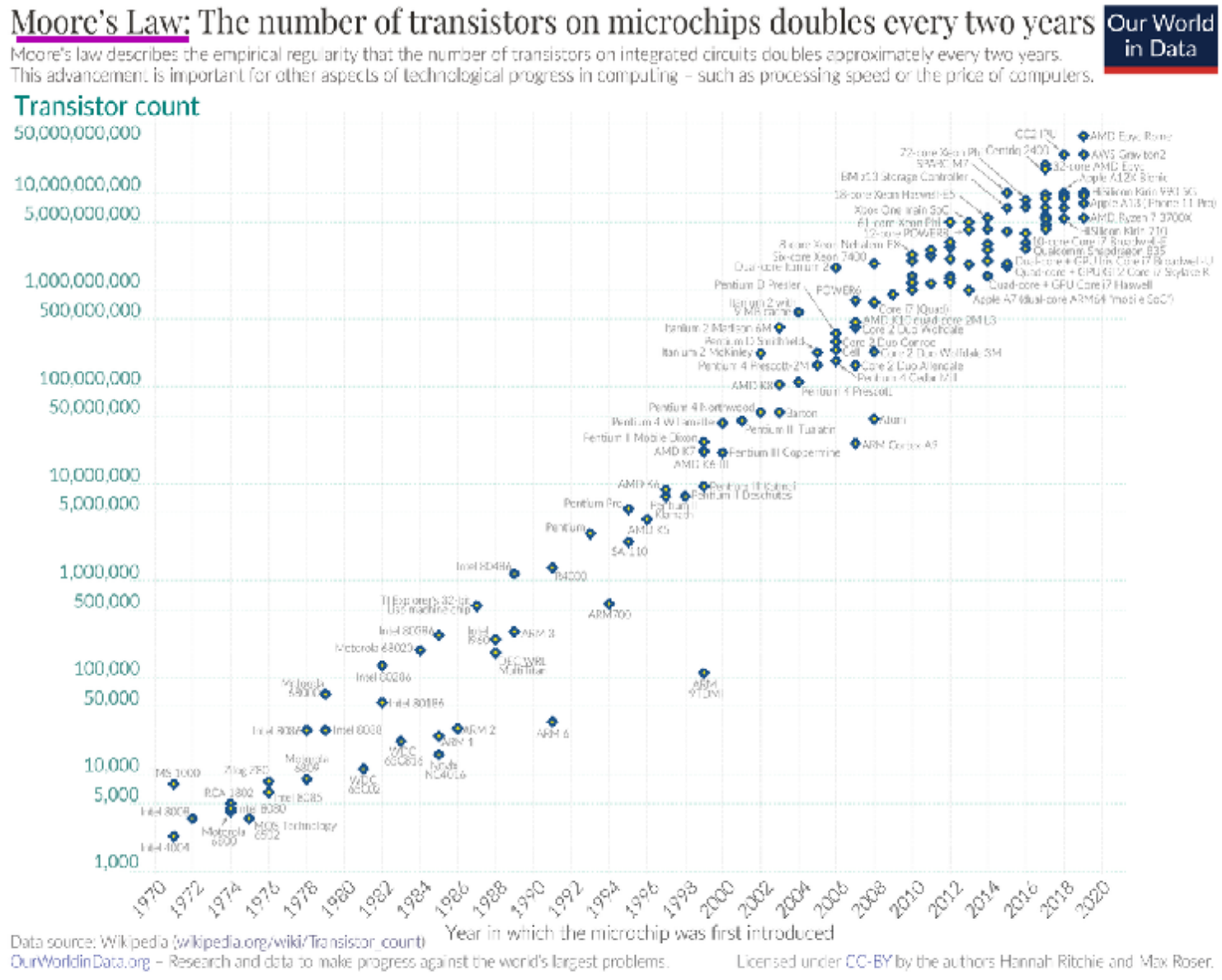
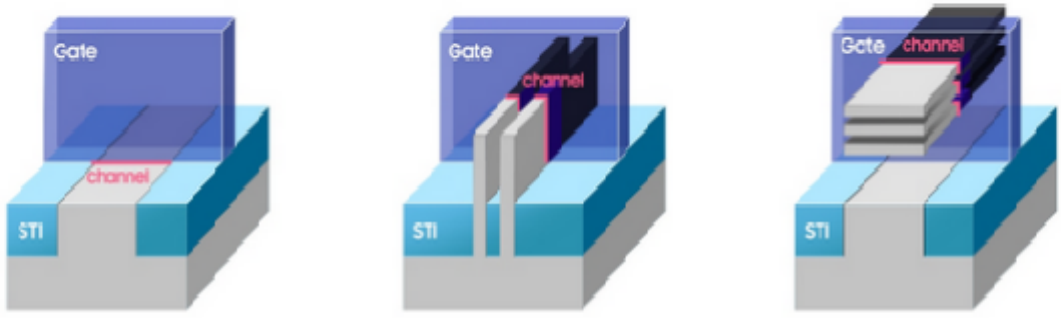
A presentation on the Photonics Days 2023
Berlin, 10.10.2023



Source: Wikipedia

Changing transistor architectures for Moore's law



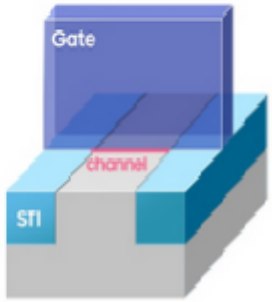
MOSFET FinFET nanosheet transistor

MBCFET

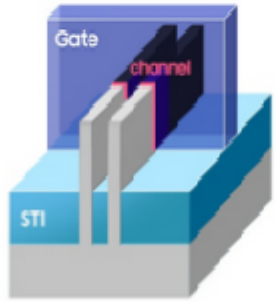
~22nm, 2011 3nm, 2022

microelectronics nanoelectronics atomar electronics?

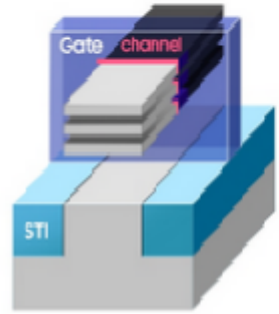
Samsung: '3nm GAA MBCFET: Unrivaled SRRAM Flexibility' Jun 21, 2023



MOSFET



FinFET



nanosheet transistor

MBCFET

alternative

SOI transistor

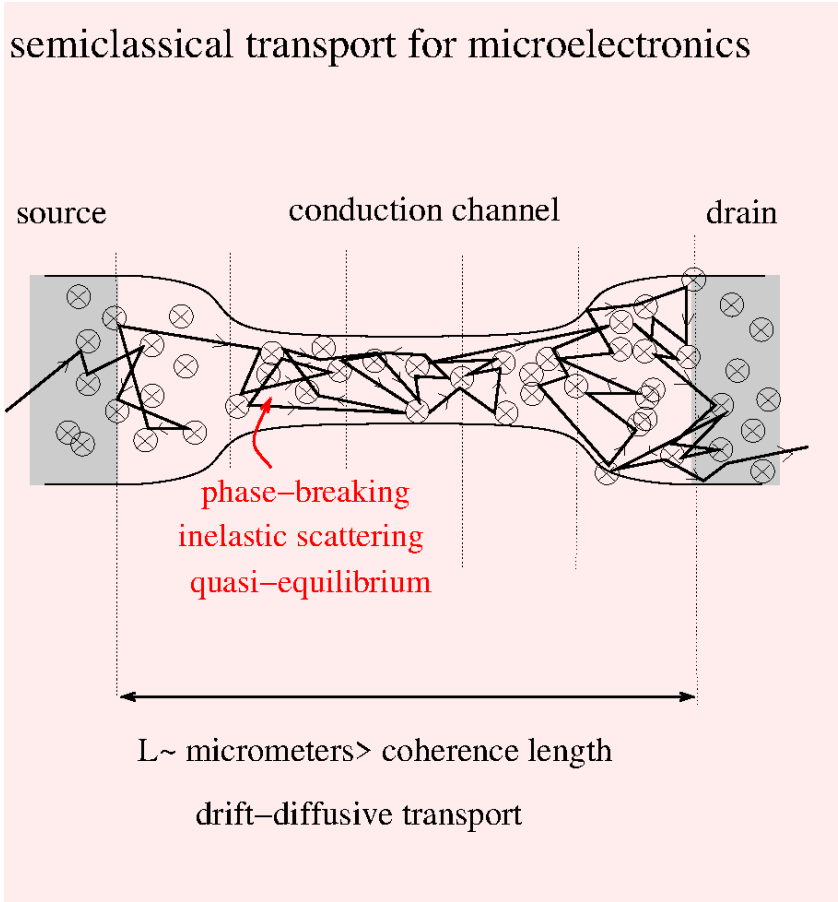
22FDX, Globalfoundries, Dresden

Two–channel transistor

resonant tunneling

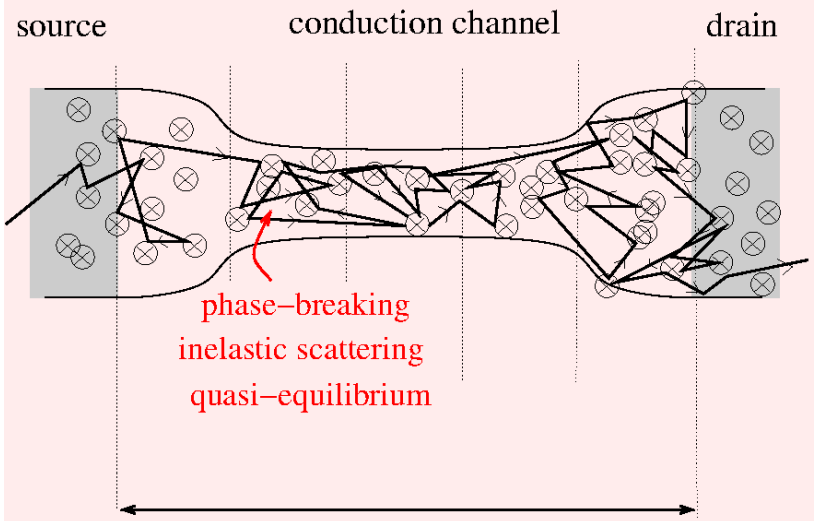
low–energy applications

Semiclassical transport vs. Quantum transport



Semiclassical transport vs. Quantum transport

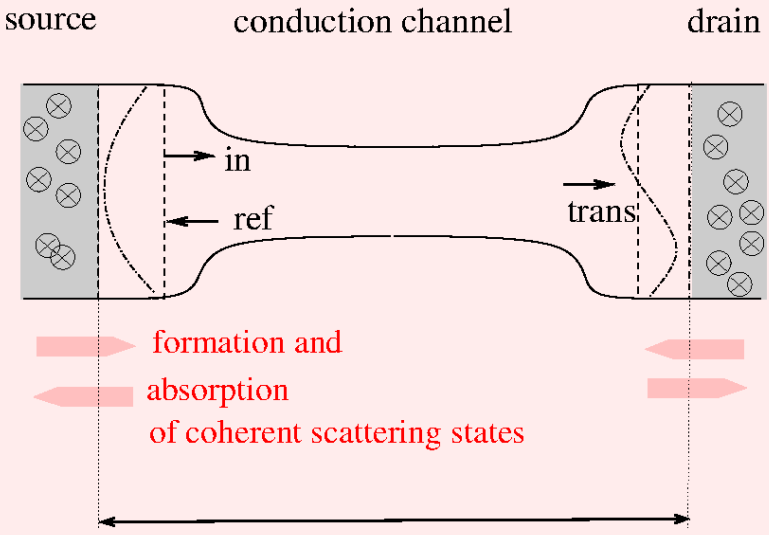
semiclassical transport for microelectronics



L~ micrometers> coherence length

drift−diffusive transport

quantum transport for nanoelectronics



L ~ tens of nms < coherence length

ballistic transport: Landauer−Büttiker formalism

1. General theory on qantum transport: Micromachines 2020, 11, 359

Article

A One-Dimensional Effective Model for Nanotransistors in Landauer–Büttiker Formalism

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2. Application to nano–MOSFETs: Mathematics 2017, 5, 68

Article

Channel Engineering for Nanotransistors in a Semiempirical Quantum Transport Model

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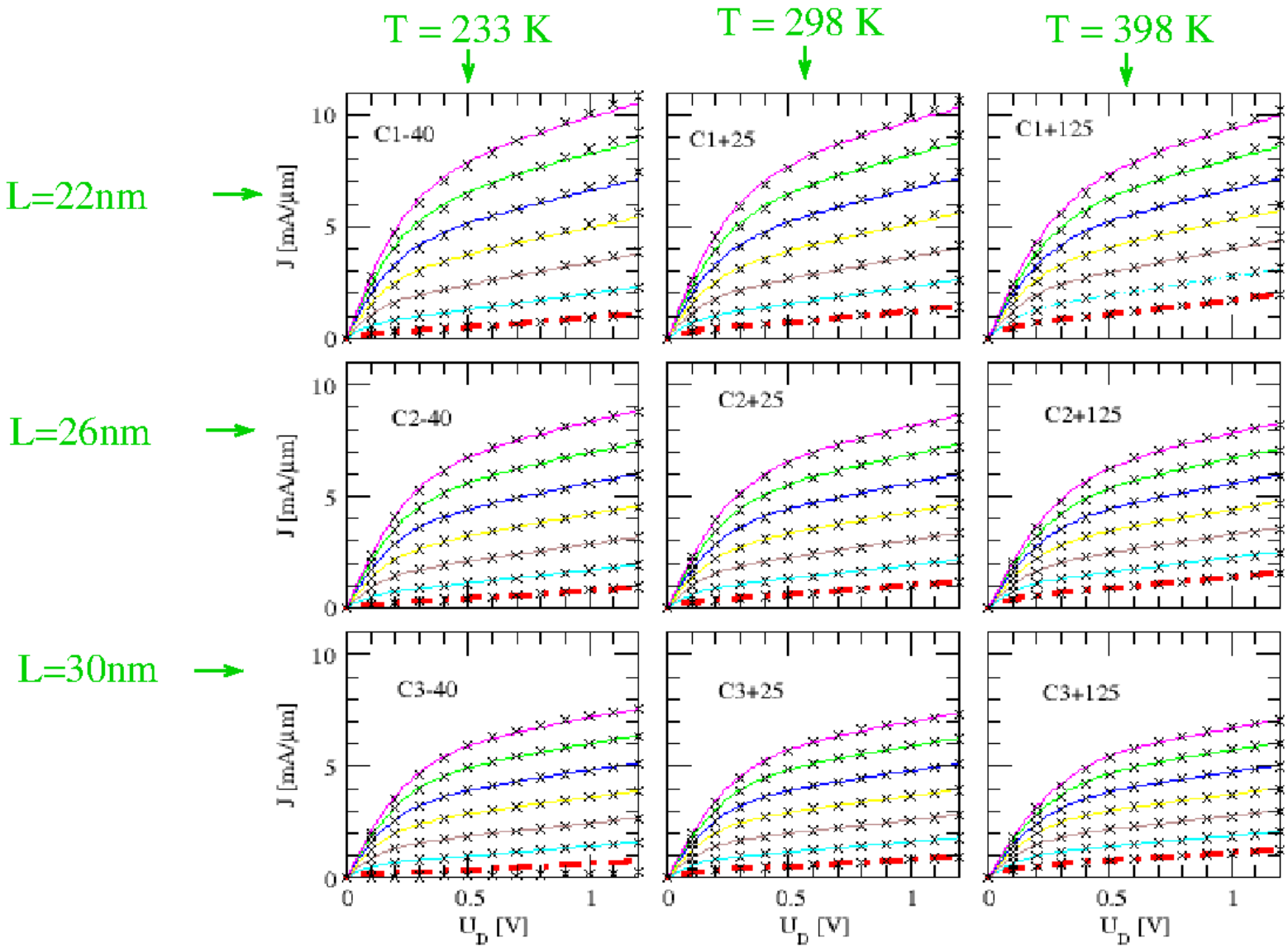
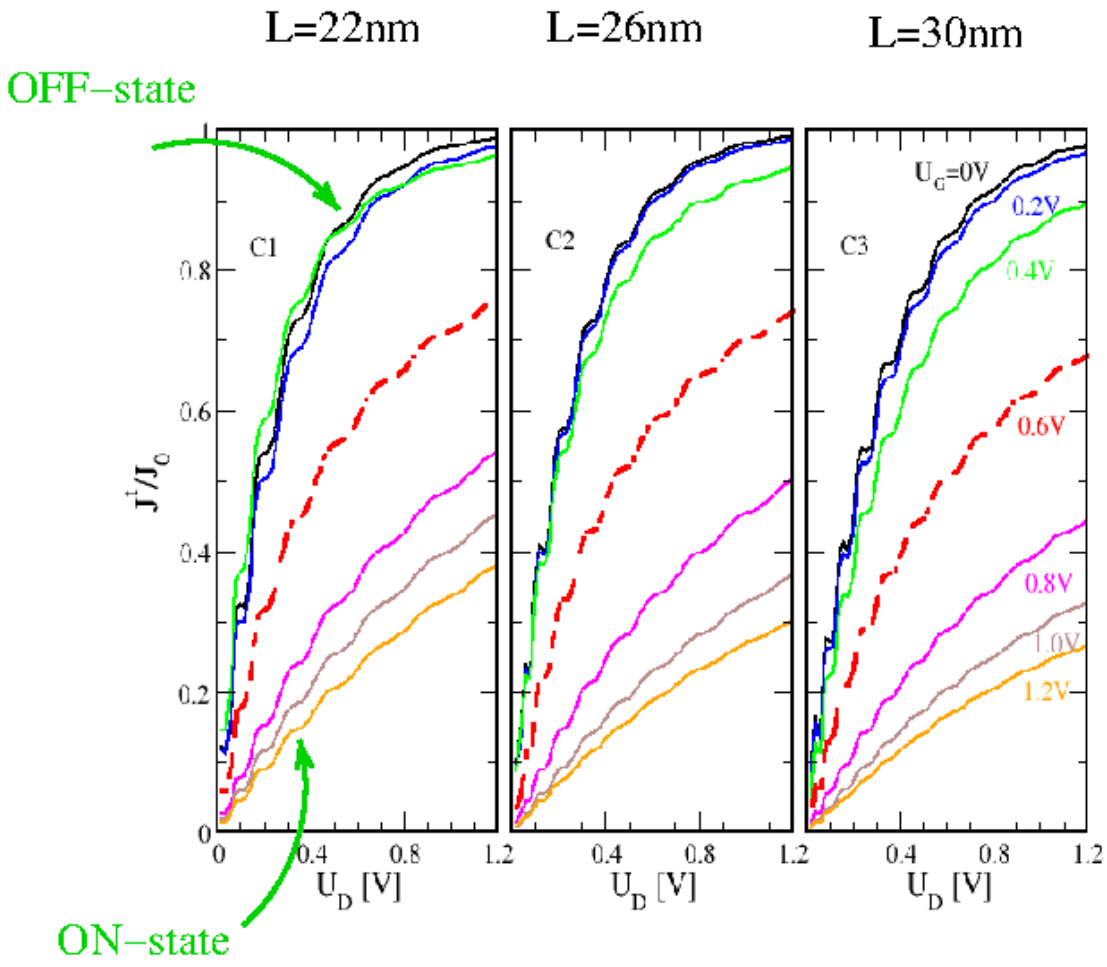
Output characteristics of nano–MOSFETs: Theory and experiment



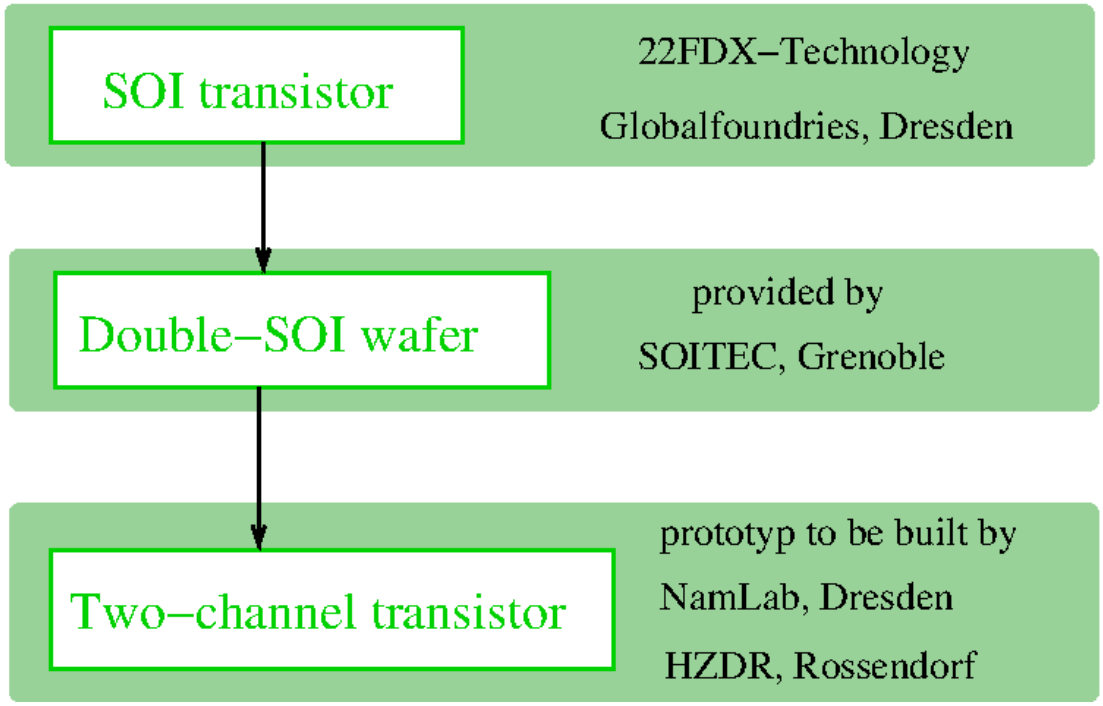
Ratio between tunneling current and total current



On the minus side : marked tunneling decreases gate control !!!

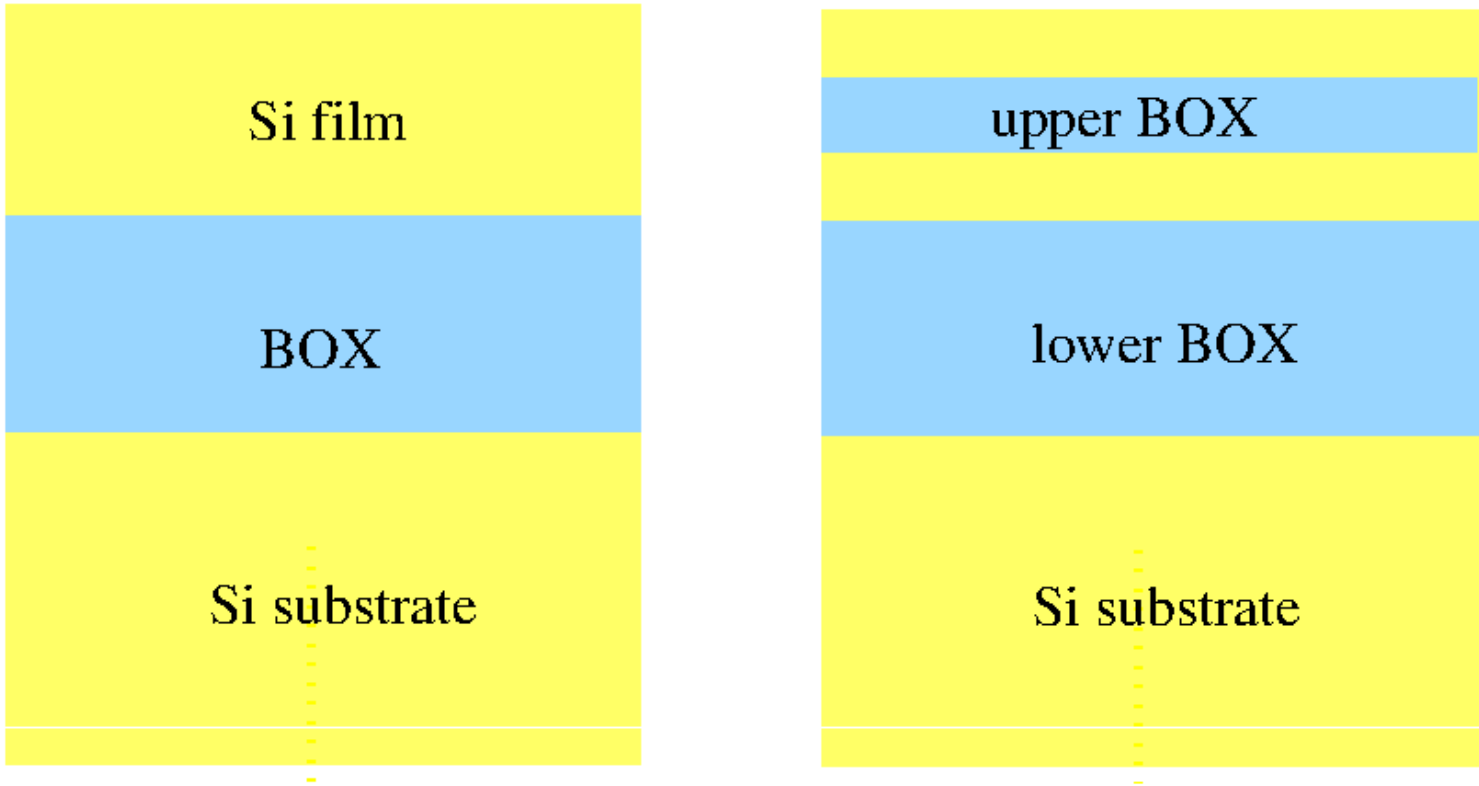
On the plus side

Tunneling as new device concept: Two channel transistor



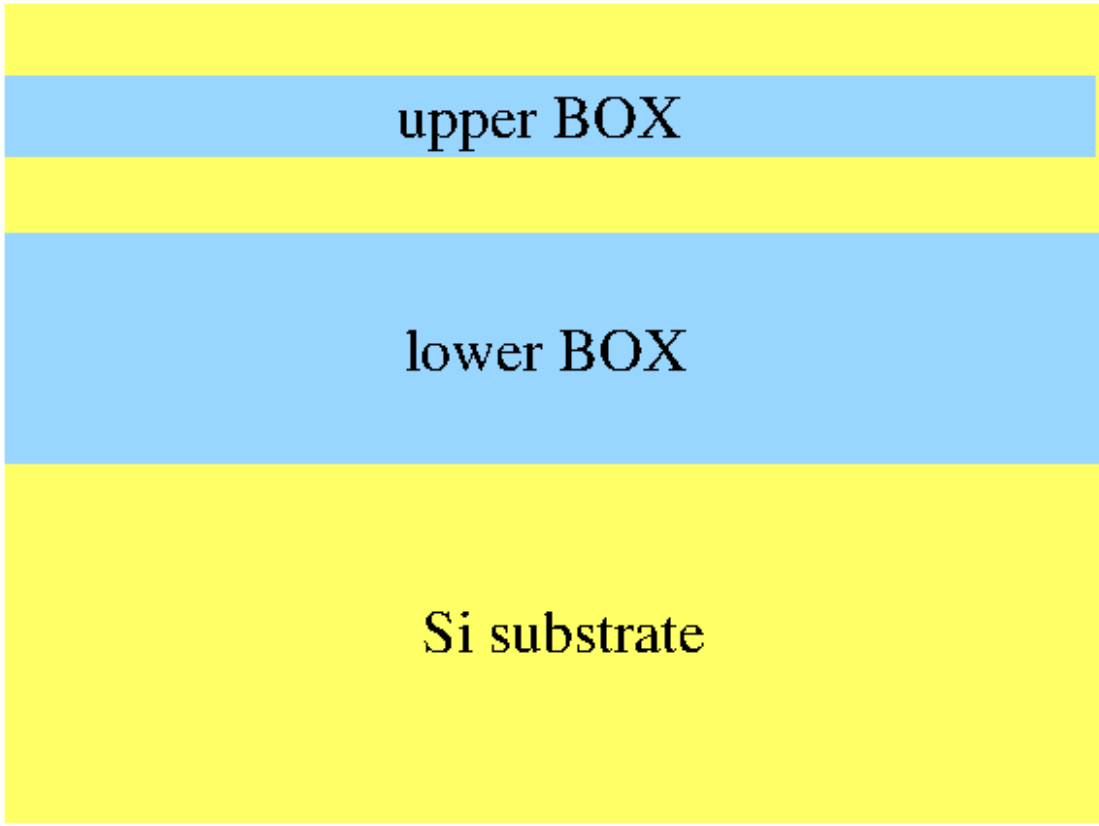
From SOI–wafer to double–SOI wafer

SOI wafer → double SOI from SOITEC (LOI)

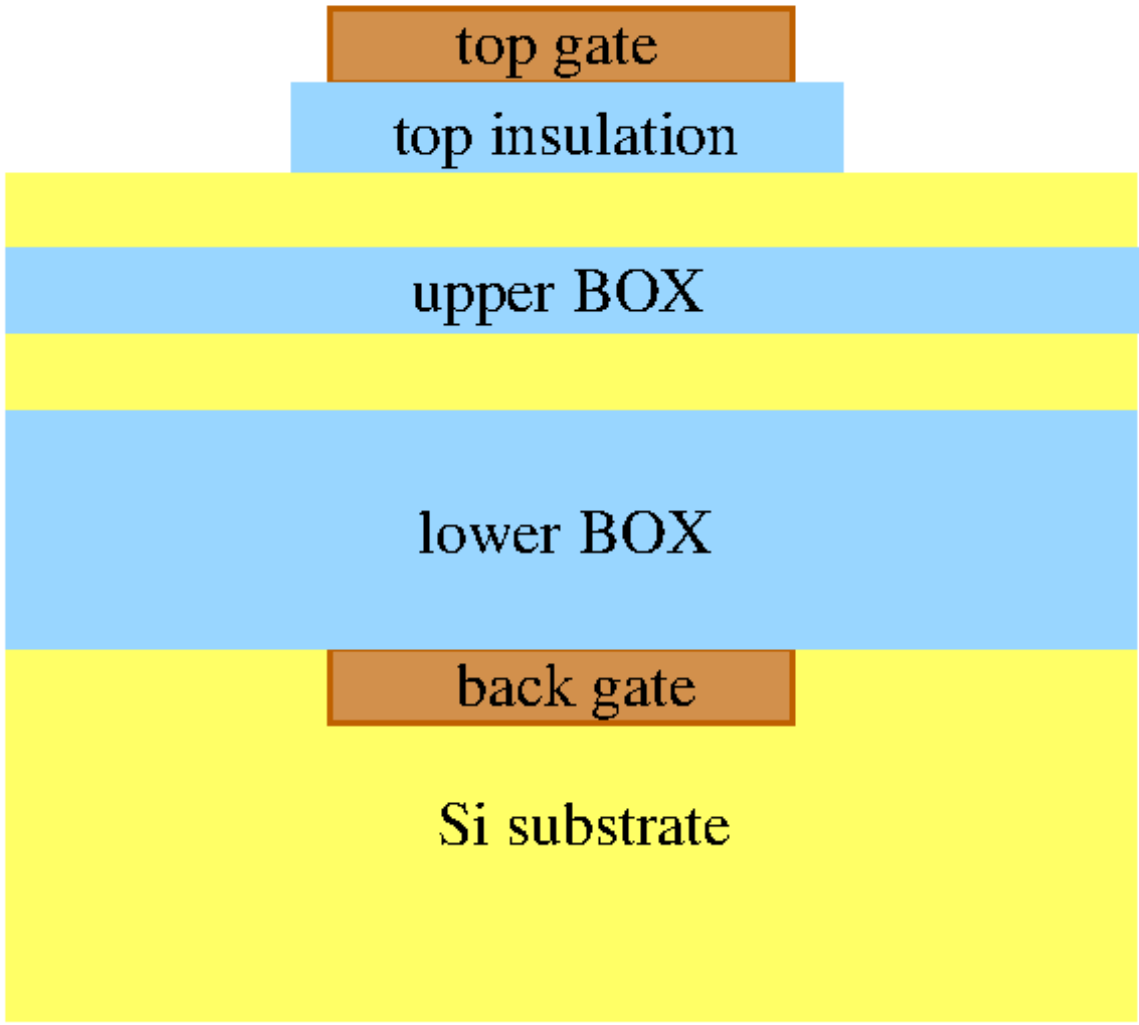


Schwarzenbach et al., 2019 IEEE SOI–3D–Subthreshold Technology Conference

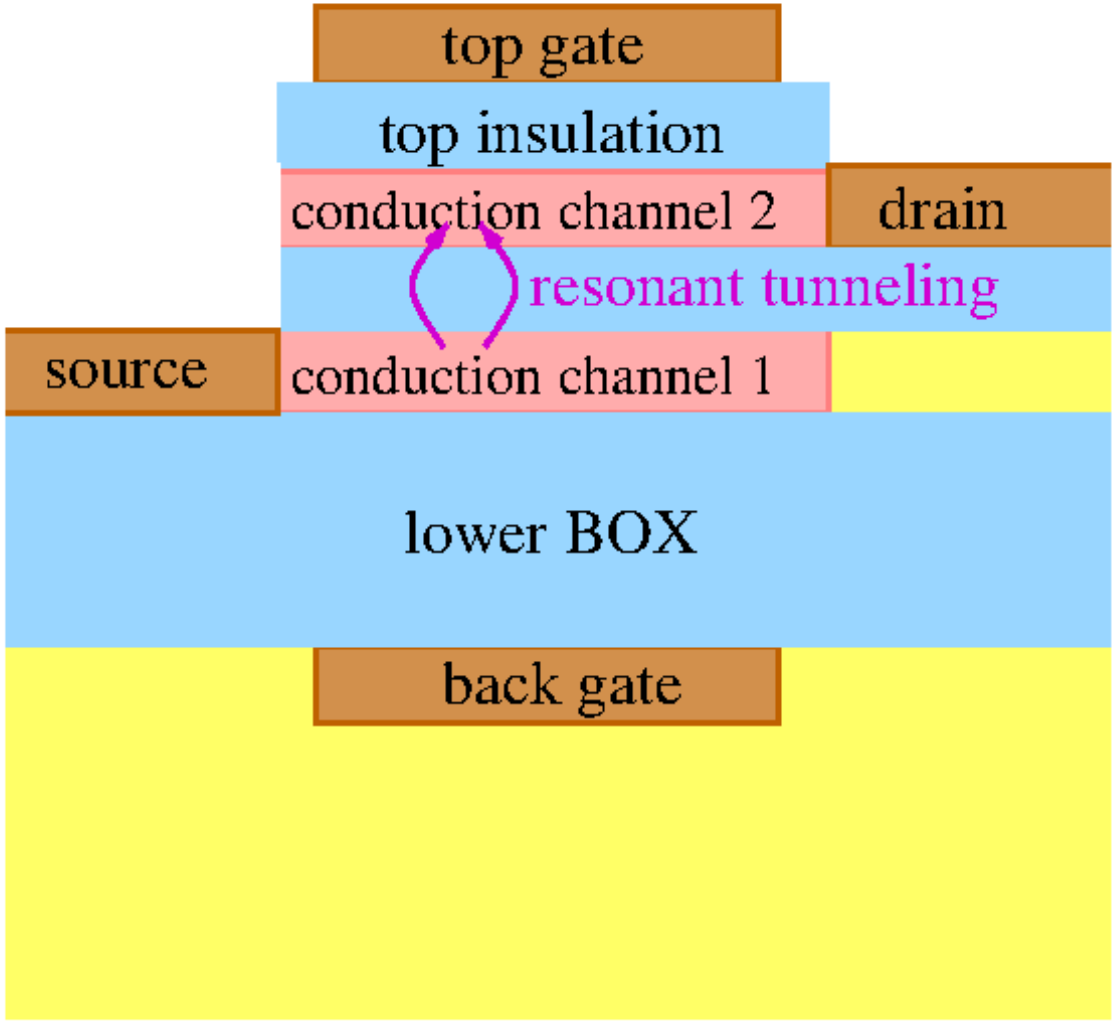
From double–SOI wafer to two–channel transistor



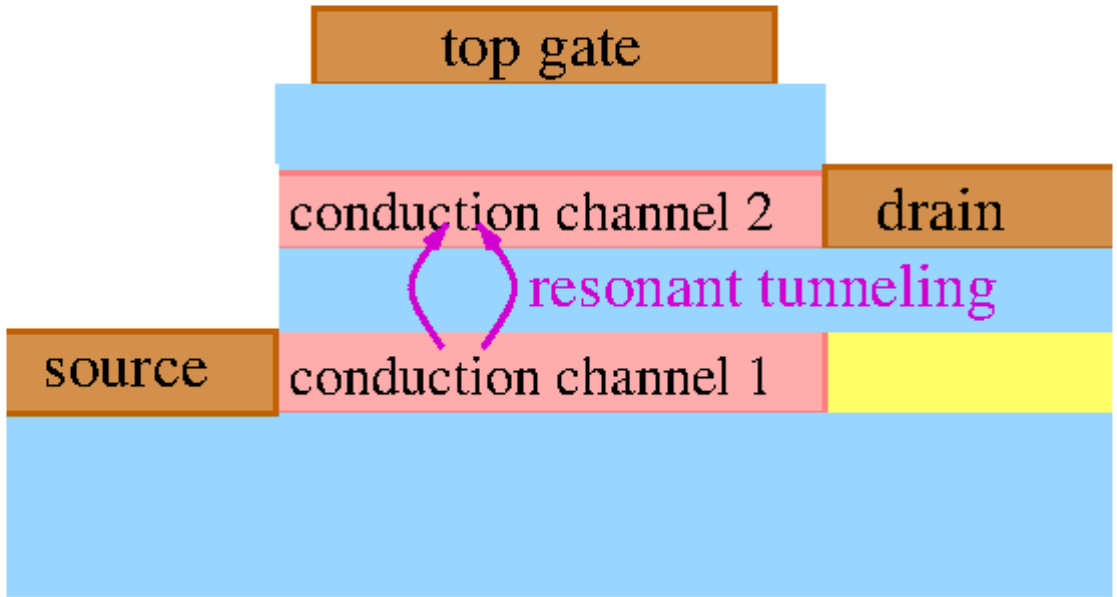
start with standard SOI–technology:

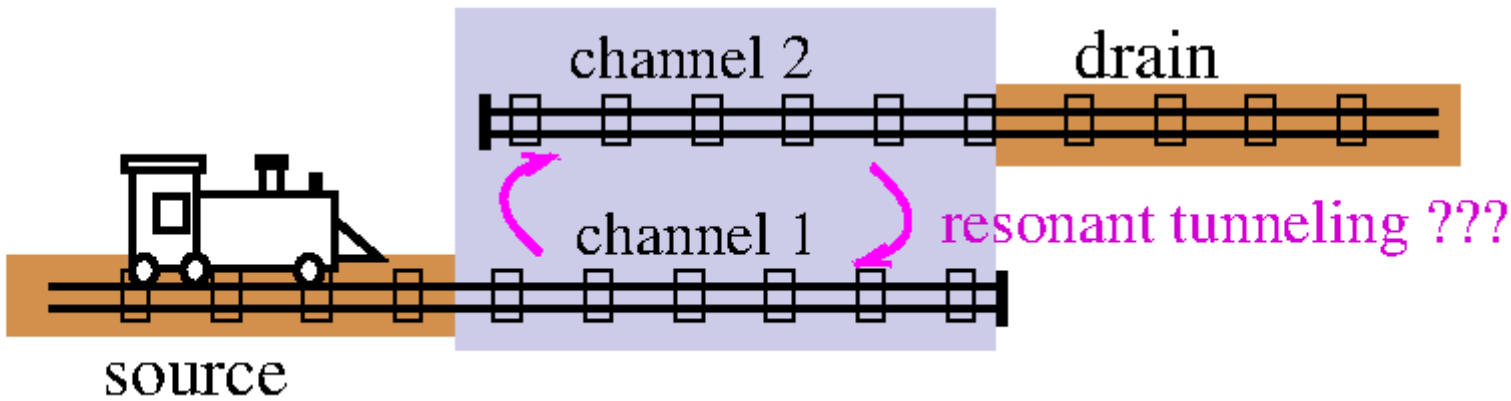


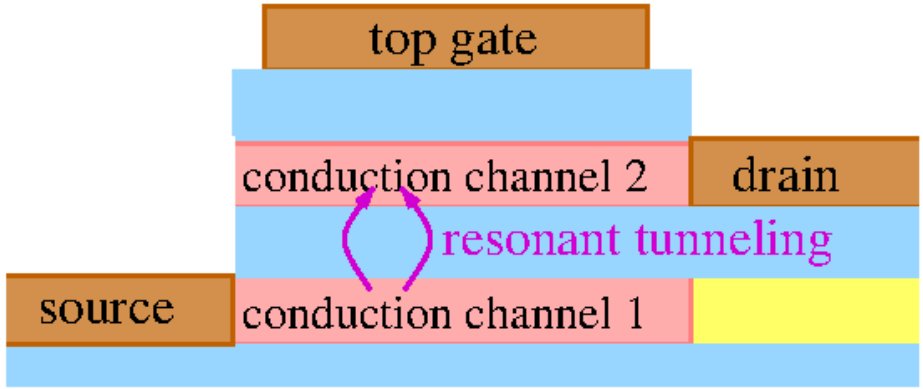
add selective source/drain contacts



functionality of the two–channel transistor

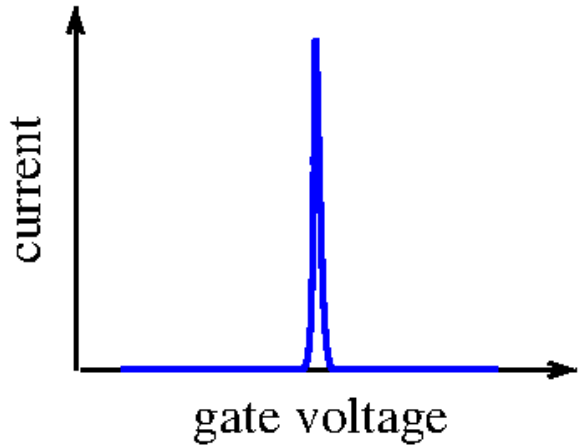


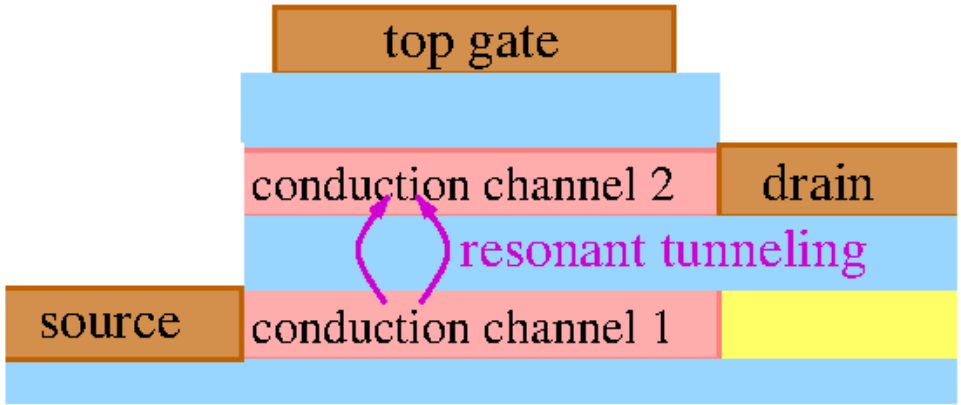


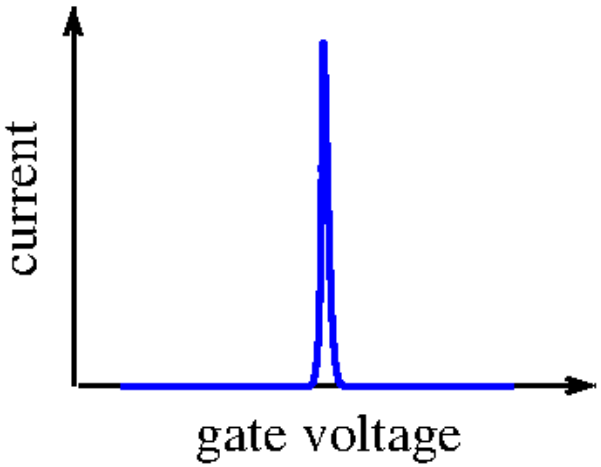


microscopic:

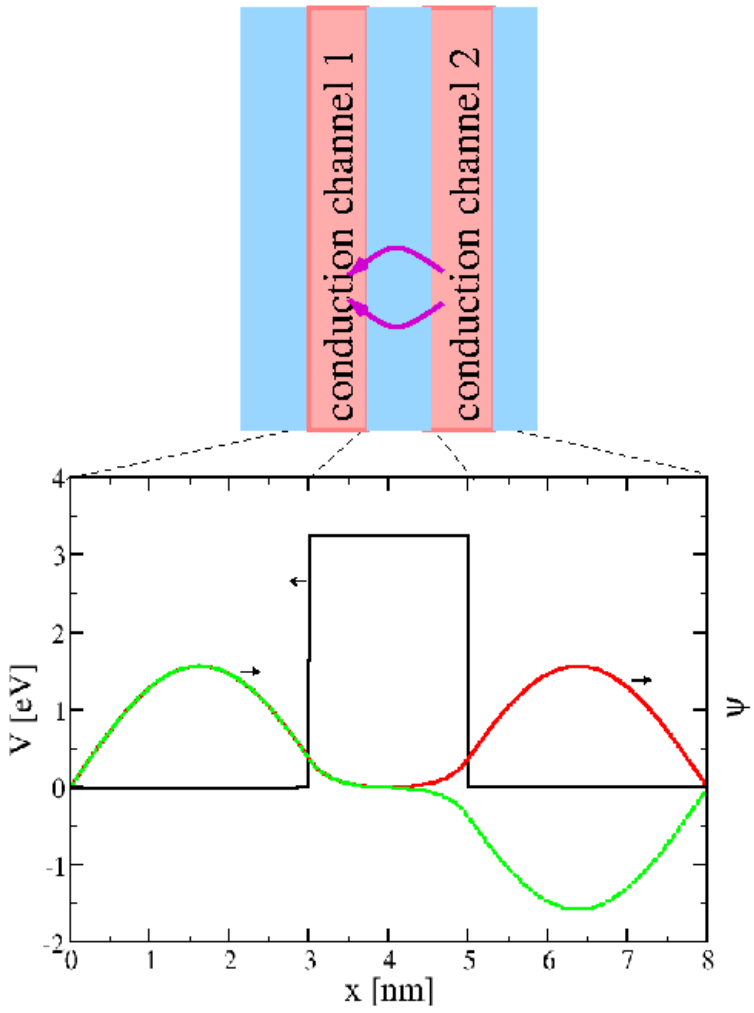
resonant tunneling peak at particular gate voltages







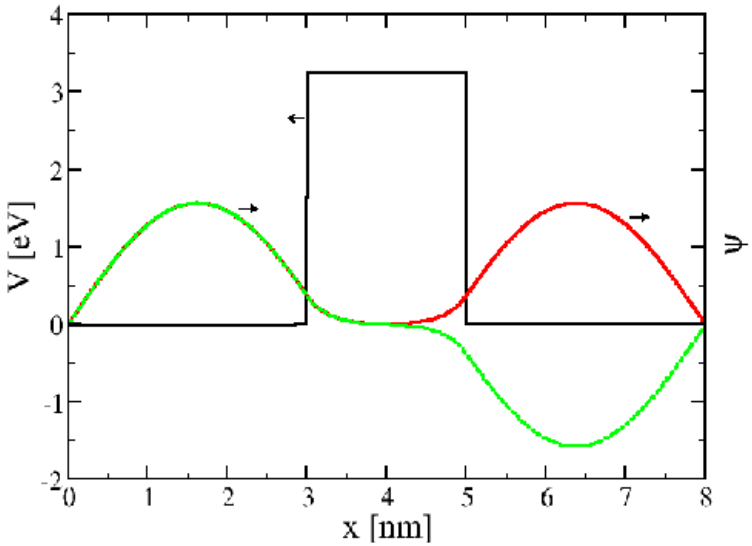
- small gate voltage ON/OFF
- low voltage / low energy
- thermal stability
- electrical engeneering CMOS–concept
  talk by G. Teepe at Photonics Days 2022
- Low temperature tunneling peak found
  in microscale GaAs Heterostructures
  (J. A. Simmons, J. Appl. Phys. 84, 5626 (1998))


conduction channel 1
conduction channel 2
V [eV]
x [nm]
ψ
4
3
2
1
0
-1
-2
0
1
2
3
4
5
6
7
8

dependence on transverse voltage = control voltage

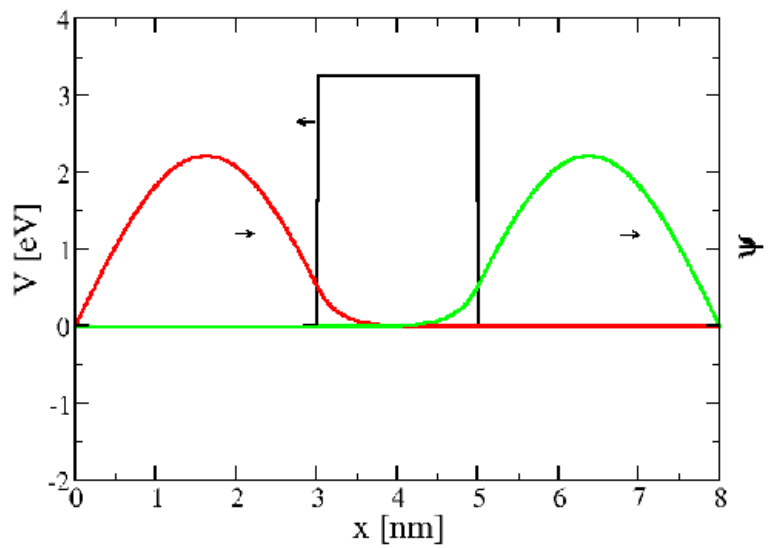
$\delta U = 0$

symmetrical potential



$\delta U = 50$ mV

asymmetrical potential



Conclusions / happy ending:

- Hope that I have convinced you that the two-channel transistor is an interesting device concept that should be given a chance.
- Best thanks for your attention !!